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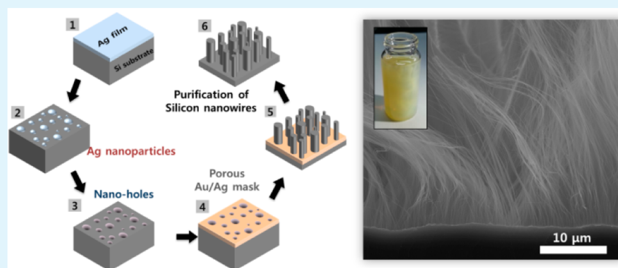
A Route for Modulating the Diameter of Cylindrical Silicon Nanowires by Using Thermal Self-Ordering Silver Nanoparticles

Sang Hoon Lee,† Tae Il Lee,† Kyeong-Ju Moon, and Jae Min Myoung*

Department of Materials Science and Engineering, Yonsei University, Seoul, Korea

Supporting Information

ABSTRACT: For the synthesis of uniform sub-80-nm silicon nanowires (Si NWs), we introduce a metal-assisted chemical etching (MCE)-based facile and high-yield route, employing simple thermal annealing and vacuum deposition processes. Under rapid thermal annealing, an ultrathin silver (Ag) film on a Si substrate is self-organized into Ag nanoparticles (NPs), which are used for making Si nanoholes through a short MCE process. After sputter deposition of Au (10 nm)/Ag (20 nm) on the caved Si substrate with nanoholes, a nanomesh is obtained. Finally, with the nanomesh as an etching mask, Si NWs are successfully produced through a second MCE process. The size of the Si NWs can be modulated by controlling the thickness of the initial Ag film. The minimum diameter of the synthesized Si NWs is 30 ± 5 nm, and the maximum diameter is 68 ± 10 nm. Furthermore, to determine the uniformity of our Si NWs, bottom-gate field-effect transistors were fabricated and the linearity of the on-current level of these transistors with the number of addressed Si NWs was confirmed.



KEYWORDS: *metal-assisted chemical etching, rapid thermal annealing, size-controllable Ag particles, Au/Ag nanomesh, Si NW transistor*

1. INTRODUCTION

Silicon nanowires (Si NWs) have received great attention as unique building blocks in future electronics by virtue of their superior properties originating from nanoscale physics or chemistry for various functional devices such as field-effect transistors (FETs),[1−4] thermoelectric cells,[5,6] solar cells,[7−11] lithium-ion batteries,[12−14] photosensors,[15] biosensors,[16−19] and light-emitting diodes.[20−22] In the past few decades, many studies on the methods for synthesizing Si NWs have been reported.[23−27]

Traditionally, a chemical vapor deposition (CVD) method based on a vapor−liquid−solid process has been used to synthesize Si NWs using nanocatalysts formed by thermal aggregation of an ultrathin noble-metal film. However, poor reproducibility in chemical composition, low production throughput, and internal metal contamination were issued as demerits in this method.

Recently, not showing these problems possessed in the bottom-up CVD method, a metal-assisted chemical etching (MCE) has been introduced by Peng et al.[28−30] and widely used for various applications[31−33] because this approach can synthesize Si NWs with high throughput and is low cost as well as easily accessible without any vacuum equipment. Unfortunately, the poor uniformity of the cross-sectional shape and diameter of the Si NWs produced using MCE, where the irregular metal catalyst nanopattern is spontaneously formed by the microelectrochemical reaction between the metal ions and Si, still remains a bottleneck in this method.

To solve this weak point, several strategies employing sophisticated nanopatterning techniques such as nanosphere lithography,[34] laser interference lithography,[35] block copolymer patterning,[36] and anodic aluminum oxide templating[37] have been proposed for modifying the original MCE process to ensure the formation of regularly patterned metal catalysts and to eventually control the size and shape of Si NWs. Although the uniformity of the Si NWs could be secured by adopting these patterning techniques, the difficulty and complexity in the nanopatterning techniques prevent the modified MCE from being used as a universal method to synthesize Si NWs in various research fields.

In this work, an MCE-based facile and high-yield route to obtain uniform sub-80-nm Si NWs, employing the self-assembly of metal nanoparticles traditionally used in the CVD method, was introduced. On the basis of two universal processes including rapid thermal annealing (RTA) and thin film deposition without any complex nanopatterning technique, our approach can be generally used by anyone who is studying Si NWs. To verify the capability of our process to produce uniform Si NWs for electronic devices, bottom-gate FETs were fabricated. The linearity of the on-current level of the transistors with the number of addressed Si NWs was confirmed. Furthermore, our method's capability of producing

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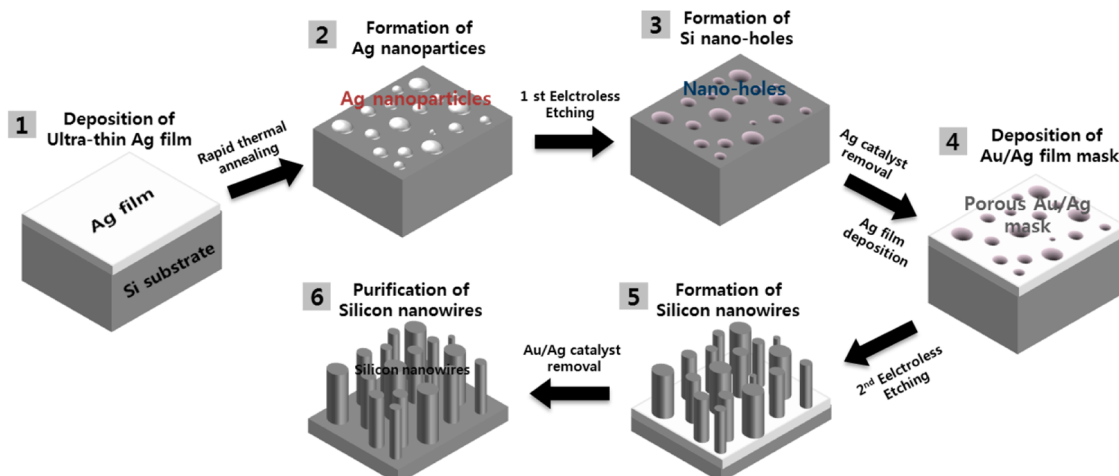
Scheme 1. Process Flow Sequence To Produce sub-80-nm Si NWs



uniform sub-80-nm Si NWs with high yield inspires the practical use of Si NWs in current and future industry.

2. EXPERIMENTAL SECTION

In general, the key demand in MCE for the synthesis of Si NWs is the formation of a silver (Ag) nanomesh consisting of separate nanoholes on a Si wafer, whose shape and diameter decide the cross section and width of the Si NWs. To create the Ag mesh, a self-organized monolayer of Ag nanoparticles (NPs) is first generated by RTA with an ultrathin Ag film, and then these NPs are converted into Si nanoholes through the first MCE process. After deposition of a gold (Au)/Ag film by sputtering, wherein the film is formed only on the flat region and not the holes, a Au/Ag nanomesh is formed. Finally, vertically aligned Si NWs are obtained by a second MCE process with the nanomesh. The entire process flow sequence is depicted in Scheme 1.

2.1. Substrate Preparation. To prepare the substrate for this experiment, Si wafers [p-type, 1−10 Ω, (100)] cut into 1.5 cm × 1.5 cm were cleaned with a piranha solution (98% H_2SO_4:60% H_2O_2 = 3:1 v/v) for 15 min and sonicated in 100 mL of deoinized (DI) water twice each for 10 min and dried by N_2 gas. In order to keep the surface characteristic formed by piranha cleaning, it was recommended to load the sample in an evaporator as soon as possible and to evacuate the chamber under 3×10^{-6} Torr.

2.2. Deposition and Thermal Aggregation of a Ag Film. The holder to which the sample was attached was rotated during e-beam evaporation, and preevaporation was performed for 10 min. Ag was deposited on the sample at a rate of 0.3 Å/s. After deposition was completed, the sample was kept in the chamber for 1 h to stabilize the Ag layer. Also, the sample had to be loaded in RTA immediately so as to minimize damage by H_2O in the atmosphere. A total of 1000 cm^3/min of H_2 gas was supplied for 15 min so that the environment was stable. Then, the temperature was increased to 700 °C at a rate of 11.46 °C/s and was maintained for 1 min in order for the Ag layer to be thermally aggregated. After RTA was finished, the Ag NPs formed were stabilized by keeping the samples in RTA with a supply of H_2 for 1 h.

2.3. Formation of Si Nanoholes. A total of 50 mL of an etching solution for the first MCE was prepared with 10% HF (50%) and 0.12% H_2O_2 (30%) and cooled from room temperature to −20 °C by a constant-temperature water bath. In case the bath was already set to −20 °C, the etching solution was frozen because of rapid cooling. The first MCE was conducted for 40 s to make 80-nm-depth nanoholes. The sample was rinsed with DI water and kept in 100 mL of 60% HNO_3 in order to remove Ag. The sample was rinsed with DI water after being kept in 60% HNO_3 for 1 h and dried with N_2 gas.

2.4. Formation of Au/Ag Nanomesh. The completely dried sample was loaded into a sputtering system, and the vacuum pressure was kept under 2×10^{-6} Torr. Ar gas was provided with 5 sccm, and the working pressure was held at 3 mTorr. Ag presputtering was performed with 22 W of direct-current (dc) power for 15 min, and Ag sputtering was conducted for 40 s. After stabilization for 5 min, Au was sputtered with 10 W of dc power for 105 s on Ag nanomesh.

2.5. Production of Si NWs. The second etching solution for Si NW synthesis was prepared with 10% HF (50%) and 0.6% H_2O_2 (30%). This solution is kept at room temperature. To obtain an intended length of Si NW, the etching time was adjusted. The sample was rinsed with DI water after the chemical reaction finished and kept in aqua regia for 1 h to remove Au and Ag.

3. RESULTS AND DISCUSSION

3.1. Self-assembly of Ag NPs. To obtain fine and clear hemispherical Ag NPs, the kinetics of formation and movement of the Ag NPs on the substrate should be controlled during the RTA process because Ag NPs given excess kinetic energy are mutually clumped together. As shown in Figure 1a, the

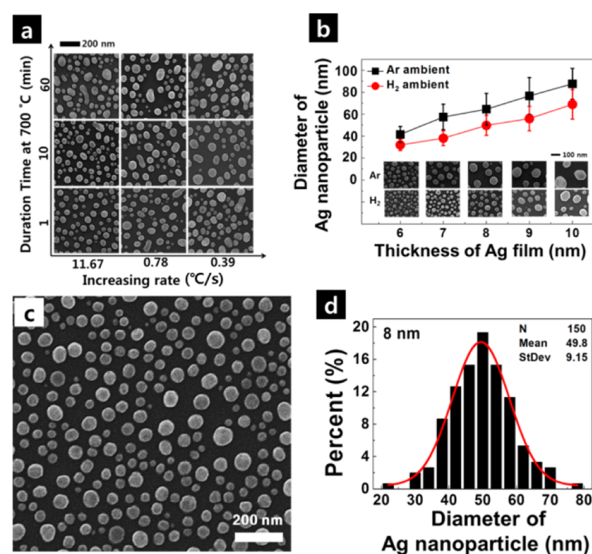


Figure 1. Ag NP formation under various conditions of RTA: (a) results of thermal aggregation of a 8-nm-thick Ag film; (b) relationship between the film thickness and NP diameter after annealing in Ar and H_2 ambience. Top-view SEM image (c) and statistical distribution of the diameters (d) of typical Ag NPs produced from an 8-nm-thick Ag film by RTA at 700 °C for 1 min with 11.67 °C/s in H_2 ambience.

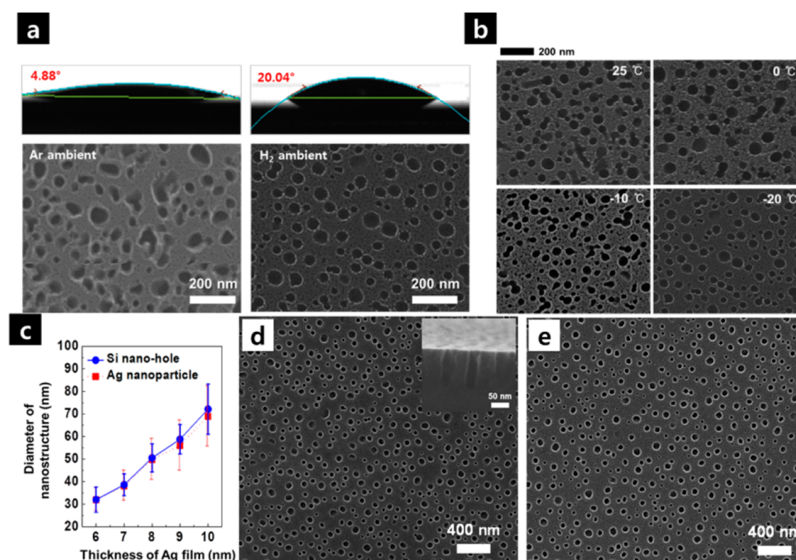


Figure 2. Si nanohole formation by partial etching (the first electroless etching): (a) contact angles on the Si surface after thermal annealing under Ar and H_2 ambience and their results of the first MCE; (b) quality of Si nanoholes according to the process temperatures; (c) statistical size comparison between the Ag NPs and Si nanoholes for various thicknesses of the Ag film; (d) top-view SEM image of typical Si nanoholes formed from the Ag NPs; (e) top-view SEM image of the porous Au/Ag film sputtered on the caved Si wafer.

increasing rate up to and duration time at 700 °C are essential variables related to the kinetics of thermal aggregation of the Ag film. For an 8-nm-thick Ag film, the optimized conditions to obtain high-quality Ag NPs were found to be 11.67 °C/s and 1 min. In fact, these conditions depend on the specification limit of our RTA system, but it is clear that, to obtain high-quality Ag NPs, the Ag film should be rapidly heated to 700 °C and then cooled to room temperature. Besides the kinetics, the surface energy of the Si substrate is a thermodynamically important factor affecting the size of Ag NPs; the lower the surface energy of the substrate, the higher the wetting angle of the Ag NPs and the smaller the NP size. Because the surface energy of a hydrogen-terminated Si substrate is normally lower than that of a native-oxide-covered substrate, the equilibrium wetting angle of the hemispherical Ag NPs should increase during the RTA process in H_2 ambience. Experimentally, the size of the Ag NPs in H_2 ambience was smaller by 20 nm than that in Ar ambience, as shown in Figure 1b. Moreover, irrespective of the type of ambient gas, as the Ag film thickness increased, the size of the Ag NPs increased linearly. On the basis of this tendency, the size of the Ag NPs is modulated as a means of controlling the diameter of the Si NWs. A typical scanning electron microscopy (SEM) image of the hemispherical Ag NPs generated from an 8-nm-thick Ag film thermally aggregated at 700 °C for 1 min, at the rate of 11.67 °C/s in H_2 ambience, is exhibited in Figure 1c. The statistical distribution of the diameters of the Ag NPs is displayed in Figure 1d. The mean diameter and standard deviation were 49.8 and 9.15 nm, respectively.

3.2. Formation of Si Nanoholes and Au/Ag Nanomesh. The most sensitive and prominent step in our process is the formation of Si nanoholes through the first MCE process, in which the key step is to obtain Si nanoholes that are similar in shape to the Ag NPs. In general, the following microelectrochemical reaction occurs during MCE: $Si + 6HF + H_2O_2 \rightarrow H_2SiF_6 + 2H_2O + H_2$. During this reaction, as Si is oxidized and gas-phase H_2 is generated at the boundary between the Ag NPs and Si wafer, the adhesion of the Ag NPs on the Si substrate becomes unstable and weak. Therefore, the Ag NPs driven by ambient thermal energy can easily move on the substrate in the lateral direction during MCE, and, consequently, distorted Si nanoholes are formed. To minimize the lateral movement of Ag NPs during the short MCE process, H_2 ambience was preferred for RTA because hydrogen-terminated Si had a lower surface energy than did Si with a native oxide layer. This was proven by the relatively high contact angle of a water drop on the Si substrate after RTA in H_2 ambience in comparison with that in Ar ambience, as shown in contact-angle images of Figure 2a. The effectiveness of lowering the surface energy in hindering the lateral movement of Ag NPs, as well as the creation of vertical Si nanoholes, could be confirmed by the results shown in Figure 2a. Many straight Si nanoholes were obtained from the Ag NPs formed by RTA in H_2 ambience, whereas distorted Si nanoholes were observed in Ar ambience. As another method of restricting the lateral movement of Ag NPs, the etching solution was cooled in order to reduce the ambient thermal energy, which is the driving force of the movement. To determine the effect of the temperature of the etching solution on the formation of Si nanoholes, MCE was conducted with an etching solution (10% HF and 0.12% H_2O_2) at various temperatures: 25, 0, −10, and −20 °C. As shown in Figure 2b, at low temperatures, vertical Si nanoholes were preferentially obtained. Under the optimized etching conditions, Si nanoholes were formed by MCE for 40 s with Ag NPs of various sizes; the results of a statistical size comparison between the NPs and nanoholes are shown in Figure 2c. The effectiveness of our optimization can be seen from the results showing nearly the same size distribution of NPs and nanoholes before and after the short MCE process. Top-view and cross-sectional SEM images of typical Si nanoholes formed by MCE with Ag NPs thermally aggregated from the 8-nm-thick Ag film are exhibited in Figure 2d, and the hole depth is determined to be approximately 80 nm from the inset image.

On a Si substrate with nanoholes, a Ag film was deposited using a dc sputtering system. A sputtering system was used instead of an evaporator so that Ag atoms could be deposited

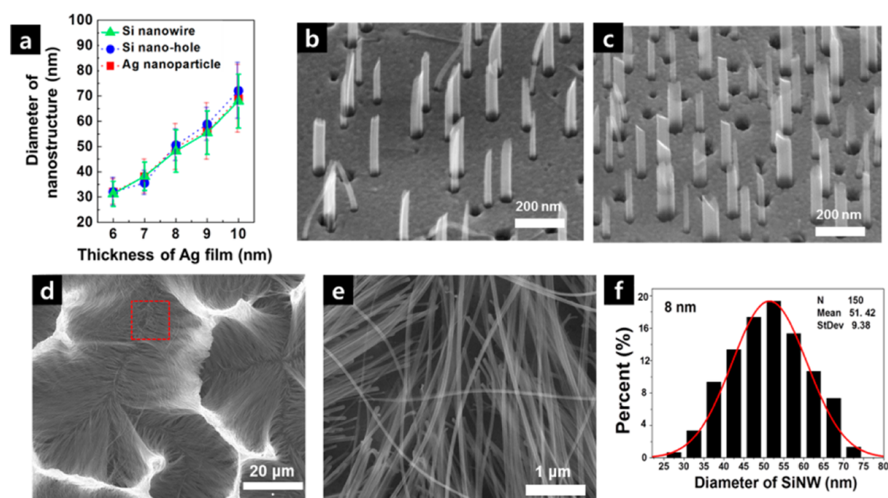


Figure 3. Formation of Si NWs by the second MCE. (a) Statistical size comparison of Ag NPs, Si nanoholes, and shortly etched Si NWs for various thicknesses of the Ag film. 40°-tilted SEM images of typical Si NWs formed from the second MCE with porous Ag films patterned by Si nanoholes for (b) 6-nm-thick and (c) 8-nm-thick films. (d) Top-view SEM image of Si NWs etched for 3 h and (e) highly magnified SEM image of the red square area in part d. (f) Statistical distribution of the diameters of the etched Si NWs for 3 h produced from a 8-nm-thick Ag film.

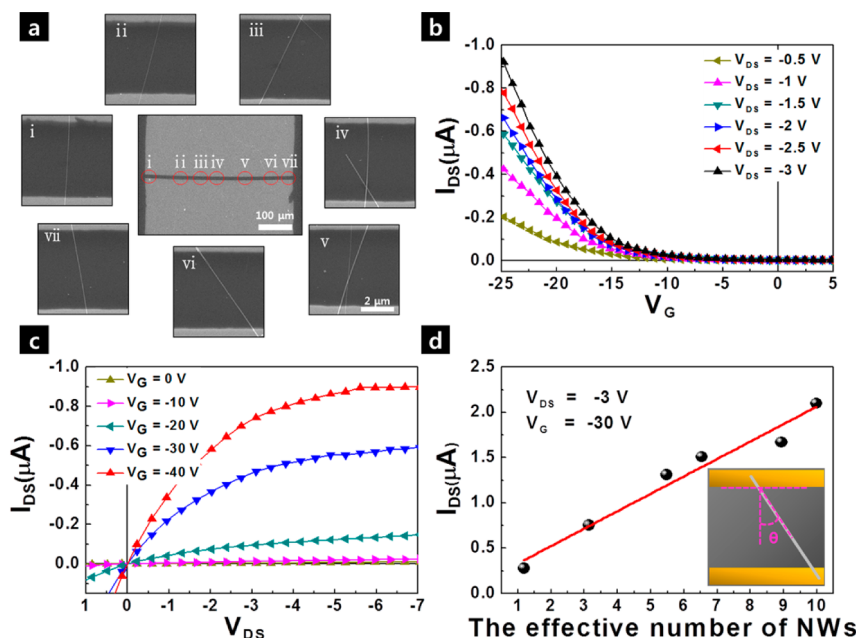


Figure 4. Si NW FET characteristics. (a) SEM images of the active layer with eight of the NWs hanging between electrodes. (b) Transfer characteristic of the fabricated transistor with eight NWs. (c) Its output characteristics. (d) Distribution of the drain currents according to the effective number of NWs at −3 and −30 V of drain and gate voltages and scheme showing the tilted angle *θ*.

only on the nonporous area of the Si substrate to obtain the Ag nanomesh; evaporated Ag atoms may fly straight and penetrate the Si nanoholes, whereas sputtered Ag atoms are scattered in a random direction from their source and can hardly enter the nanoscale holes. The Ag deposition time during sputtering was adjusted appropriately because, at a very long deposition time, small holes were entirely covered with the Ag film, whereas at a short deposition time, the Ag film became discontinuous (Figure S1, Supporting Information). Au thin film was sputtered on a flat area of Ag nanomesh to reinforce the weak cohesion of Ag. A top-view SEM image of a typical porous Au (10 nm)/Ag (20 nm) film deposited on partially etched Si by MCE with Ag NPs thermally aggregated from the 8-nm-thick Ag film is shown in Figure 2e.

3.3. Synthesis of Si NWs. Finally, the Si NWs were produced using a second MCE with the Au/Ag nanomesh. The conditions used in this step were the same as those used in the previous etching step, except for both the concentration of H_2O_2 and temperature of the etching solution; the second MCE was conducted using a solution of 10% HF and 0.6% H_2O_2 at room temperature. The etching rate is normally proportional to the concentration of H_2O_2. It is advantageous to use a high concentration of H_2O_2 in order to obtain straight Si NWs. However, with a single layer of Ag, the Ag nanomesh was physically peeled off by the H_2 bubbles as the etching rate increased. At H_2O_2 concentrations exceeding 0.3%, the rate of volume growth of the H_2 bubbles was higher than the rate of escape of the bubbles from the Ag/Si layer interface so that the

Ag nanomesh was separated from the Si substrate. However, the Ag catalyst could endure this damage because Au with strong cohesion characteristics was additionally sputtered on the porous Ag layer, which made nanomesh not peeled off during etching at 0.6% H_2O_2 and kept its initial shape until the end of the process. Figure 3a shows a statistical size comparison of the Ag NPs, Si nanoholes, and shortly etched Si NWs for various thicknesses of the initial Ag film. The diameter distribution of the short Si NWs was similar to that of the Ag NPs and the Si nanoholes. The minimum diameter of the synthesized short Si NWs was 30 ± 5 nm, and the maximum diameter was 68 ± 10 nm. 40°-tilted SEM images of the typical short Si NWs formed from the second MCE for 40 s with porous Au/Ag films patterned by Si nanoholes for initial Ag film thicknesses of 6 and 8 nm are exhibited in Figure 3b,c.

To obtain Si NWs with a high aspect ratio, the second MCE was carried out for 3 h using a porous Au/Ag film patterned by Si nanoholes for an initial Ag film thickness of 8 nm, and as a result, about 40-μm-length and 50-nm-diameter Si NWs were obtained with high yield, as shown in Figure 3d,e. The NWs tangled like hair due to capillary force by drying them. Also, the diameter of the NWs was perfectly kept until the end of the etching process, as shown in a highly magnified SEM image (Figure 3e). To show the statistical distribution of the diameter of Si NWs in our process, we got 150 Si NWs and the distribution of their diameters is indicated in Figure 3f; the mean diameter and standard deviation were 51.42 and 9.38 nm, which exactly matched those of Ag NPs. A typical transmission electron microscopy (TEM) image of a Si NW cut and put on a grid is presented (Figure S2, Supporting Information). From the bright-field image, the exact diameter of the Si NW was measured to be 52.02 nm. The longitudinal direction of the NW was confirmed to be ⟨100⟩ on the basis of the selected-area electron diffraction pattern (Figure S2a, Supporting Information) and the high-resolution TEM image (Figure S2b, Supporting Information).

3.4. Uniform Si NW Thin-Film Trasnsistors. To verify the capability of our process to produce uniform Si NWs for electronic devices, bottom-gate FETs were fabricated. After cutting Si NWs from a substrate and dispersing them in 99.9% C_2H_5OH, the Si NW solution was flown on a 30°-tilted thermally oxidized Si wafer (300 nm of SiO_2), modifying the previous method.[38] The device was completed by defining Au electrodes with a 5 μm stencil mask on it (Au was deposited in 100 nm by an e-beam evaporator). From the top-view SEM image of the device, the active channel width and length of all samples were confirmed. Current−voltage ($I-V$) characteristics were measured by using an Agilent semiconductor parameter analyzer (model 4145B), with contacts to the devices made by using a probe station (Desert Cryogenics, model TTP4). Figure 4a shows typical SEM images of a FET consisting of the eight Si NWs. Its p-type enhanced mode transfer characteristic when the drain voltage was changed from −0.5 to −3 V is shown in Figure 4b. Its output characteristic ($I_{ds}-V_{ds}$) is also shown in Figure 4c as a function of the gate voltage. The output characteristics represent a good ohmic electrical connection. The linearity of the on-current level of the transistors with the number of addressed Si NWs was determined. Six transistors were comparatively tested for this purpose, and the average on/off ratio of $10^{3.05\pm0.15}$ was obtained, with a threshold voltage (V_{th}) of −16.35 ± 0.35 V. As shown in Figure 4a, the channel length of each Si NW was longer than that of the gap between electrodes.

To calculate the electrical transporting characteristics of each device, the total numbers of Si NWs were estimated by considering the different lengths of the NWs. The effective number of addressed NWs was defined by $\sum_i \cos\theta_i$ (Definition S1, Supporting Information), where θ_i is the tilted angle of the ith Si NW from a perpendicular line between electrodes. The p-type linear field-effect mobility (μ_h) of each device was calculated as $\mu_h = L/(WC_dV_{ds})g_m$, where L (=5.657 μm) is the gap size between electrodes, W is the channel width of the device (=mean diameter of NWs × effective number of NWs), C_d represents the capacitance per unit area of the gate dielectric, and g_m is transconductance. C_d was measured as 12 nF/cm^2. The mobility μ_h was then determined to be 46.129 cm^2/V·s. Finally, the linear increasing of the on-current level according to the effective number of addressed Si NWs at fixed drain and gate voltages of −3 and −30 V is observed, as shown in Figure 4d. This linearity indicates that the Si NWs produced through our method have uniform diameter and surface properties.

4. CONCLUSION

In summary, an MCE-based facile and high-yield synthesis route to uniform sub-80-nm Si NWs was developed, employing RTA and thin-film deposition. Two-dimensional initial ultrathin Ag films with various thicknesses were first deposited on a Si wafer using an e-beam evaporator, and then each film was converted into zero-dimensional Ag NPs by thermal aggregation during RTA at 700 °C for 1 min, at a rate of 11.67 °C/s in H_2 ambience. After a short MCE process for 40 s at −20 °C, the Ag NPs on a Si substrate formed many 80-nm-deep Si nanoholes having the same diameter. A Au/Ag nanomesh was formed as an etching mask on the caved Si substrate with nanoholes, by sputter deposition for 40 and 105 s, respectively. Finally, Si NWs of various sizes were produced by the second MCE at room temperature with the Au/Ag nanomesh. The size of the holes on this nanomesh could be easily modulated by changing the thickness of the initial Ag film because the size of the Ag NPs linearly increased with the thickness of the initial Ag film; furthermore, the cross sections of the Si nanoholes were created in the same manner as those of the Ag NPs. The minimum diameter of the synthesized Si NWs was 30 ± 5 nm, and the maximum diameter was 68 ± 10 nm. To confirm the capability of our synthesis route, vertically aligned 40-μm-long Si NWs with a high aspect ratio (~800) were produced via a 3 h MCE process, and their dispersion, crystallinity, and longitudinal direction were determined. Furthermore, the uniform quality of synthesized Si NWs was verified by the linearity of the on-current level of the transistors with the number of addressed Si NWs. The proposed approach affords uniform, diameter-controlled and high-yield Si NWs by simple traditional processes, proving that MCE can be used as a universal method to get high-quality Si NWs for various applications that require a large number of sub-80-nm Si NWs with the same crystal direction and chemical composition.

■ ASSOCIATED CONTENT

Supporting Information

Results of the excess and less deposition of the Ag film, TEM analysis of Si NWs, and the effective number of NWs. This material is available free of charge via the Internet at http://pubs.acs.org.

AUTHOR INFORMATION

Corresponding Author

*E-mail: jmmyoung@yonsei.ac.kr.

Author Contributions

†These authors contributed equally.

Notes

The authors declare no competing financial interest.

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